A Report on a Two-day National Symposium on
Heterogeneous Computing: Platforms, Tools and Applications

Organized by the Departments of ECE and CSE, UCE(A), OU in collaboration with AMD India and supported by the OU ECE Alumni Association (OUECEAA) held during August 31 and September 1, 2012 at IETE, OU Campus, Hyderabad, AP

The Symposium was started with the lighting of the lamp ceremony followed by invocation. Subsequently inaugural function took place for an hour. Prof R Rameshwar Rao, Honorable Vice Chancellor of JNTUH, Hyderabad was the Chief Guest and Mr Manoher Bommena, Site Head, AMD Hyderabad was the Guest of Honor. Prof Sameen Fatima, HOD, CSE Dept., UCE gave the welcome address and Prof S Ramachandram, Vice Principal, UCE briefed about the symposium. Mr. Manoher Bommena said that almost all the top 10 semiconductor companies are having their research and development centers in India. Further we have to plan to make the India not only the semiconductor design center, but also have to see that India can become product conceptualization center. Prof Rameshwar Rao explained in brief the history and importance of heterogeneous computing and Open Computing language (OpenCL). Prof VSS Kumar, Principal, UCE (A), OU presided over the function. Mrs K Shyamala, Coordinator for the symposium, CSE Dept., UCE gave vote of thanks. Prof DVR Vithal (retired), Patron, OUECEAA and Prof K Kishan Rao, President, OUECEAA also graced the occasion.

Fig 1 Lighting of the lamp by Prof R Rameshwar Rao, VC, JNTU-H

Fig. 2 Invocation by BE, ECE students

The key note address was delivered by Mr. Manoher Bommena. He gave a talk on **A New Era of Computing.** Diminishing returns in the single-core and multi-core arena led AMD to be at the forefront of the fusion innovation, creating what we today call the **Accelerated Processing Unit (APU).** He also explained the need of **Heterogeneous System Architecture (HSA)** and touched upon the HSA Foundation (HSAF) which was formed by AMD, TI, ARM etc.

Fig. 3 Participants of inaugural function

Fig. 4 Mr. Manoher Bommena, Site Head, AMD, Hyd.

Dr K Srinidhi, Director, Product Application Engineering, AMD gave a talk on **Programming in a Heterogeneous World.** In today's world of diverse applications and platforms one single processor CPU or GPU or FPGA won't fit and it is important to find the right tool for the right job. Heterogeneous computing addresses this limitation and opens the platform to drive developer innovation.

Fig. 5 Dr K Srinidhi, Director, Product Apps Engg., AMD

Fig. 6 Participants of felicitation function

Later Prof Rameshwar Rao (Alumnus of the ECE Dept., UCE, OU) was felicitated, on the occasion of his superannuation from service to Osmania University. Prof S Satynarayana, Honorable Vice Chancellor, OU was the Chief Guest of this function. Many stalwarts (Rector and Registrar of JNTU, Directors of JNTU and OU centers) also attended. Prof Satynarayana was appreciative of the contributions made by Prof Rameshwar Rao to OU. He also wished him great success with JNTU-H. Prof Rameshwar Rao expressed his happiness and satisfaction over serving Osmania University with full cooperation from the staff and administration of the OU. He has recollected the efforts and affection shown on him by the senior professors like Late Prof KK Nair (founder Head, ECE Dept., UCE), Prof Alladi Prabhakar (former Principal, UCE), Prof DVR Vithal (former Director, OU Computer Center) and Prof DC Reddy (former VC of OU). Mr B Rajendra Naik, Coordinator of the symposium, ECE Dept., gave the vote of thanks.

Fig. 7 Address by Prof S Satyanarayana, VC, OU

Fig. 8 Prof R Rameshwar Rao, VC, JNTUH being felicitated

After the lunch break there were two talks covering the basics and giving an overview of OpenCL and AMD Application Software Development Kit (SDK). Prof S Ramachandram, CSE Dept., UCE gave a talk on **Overview of Open Computing Language (OpenCL).** OpenCL is a framework for writing programs that execute across heterogeneous platforms consisting of central processing unit (CPU), graphics processing unit (GPU), and other processors. OpenCL includes a language for writing kernels (functions that execute on

OpenCL devices), plus application programming interfaces (APIs) that are used to define and then control the platforms. OpenCL provides parallel computing using task-based and data-based parallelism.

Mr Sushant Kumar & Mr Srinivasulu Charupally, software engineers, AMD gave a talk on **Parallel Programming with OpenCL and AMD APP SDK Tools**. AMD APP SDK is a complete development platform created by AMD to quickly and easily develop applications accelerated by AMD APP technology. The SDK allows programmers to develop applications in a high-level language, OpenCL™.

On the second day, before lunch, four lectures were delivered covering hardware tools from various vendors and applications using different processors/tools.

Dr K Pramod Kumar, Division Head HPC, Dept. of Space (ISRO), ADRIN, India gave a talk on **Heterogeneous Computing Platforms Used in Satellite Data Processing to Achieve High Performance.** He described the issues and complexities involved in satellite data processing and use of heterogeneous platforms– FPGAs, GP/GPUs and multicore CPUs for overcoming the data exodus and also achieving High Performance. Use of Open Standards minimizes many of the issues such as hardware and software integration, programming complexity, debugging and maintenance.

Mr K Ananda Babu, Scientist E, ANURAG, DRDO, gave a talk on **Reconfigurable Computing Platforms for Embedded Systems.** He had explained importance of single portable computing device for all needs of a soldier. It is preferable to use the same computing device for communication, computation, position location etc. Reconfigurable FPGA can be used as computing device for these applications. He had explained applications of FPGA for face recognition which requires large number of computations.

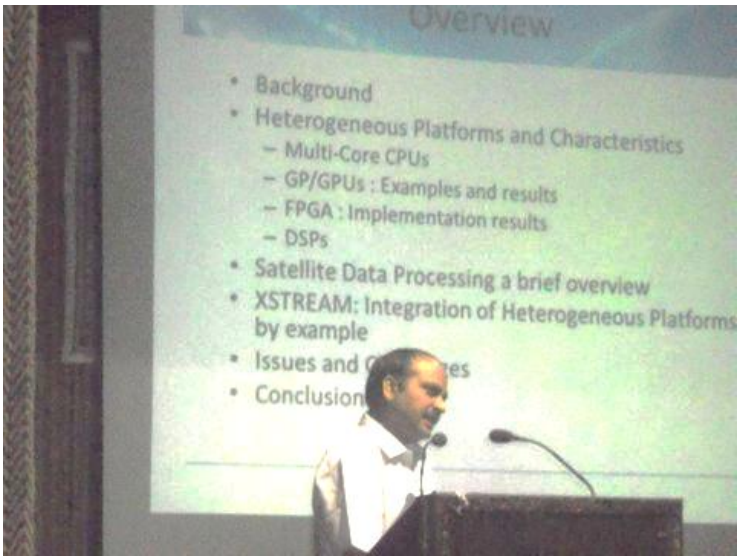

Fig. 9 Dr K Pramod Kumar, ADRIN (ISRO), India

Fig. 10 Mr. K Ananda Babu, ANURAG (DRDO), India

Mr Rajesh Mahapatra, Senior Engineering Manager, Analog Devices gave a talk on **Efficient Hardware Software Partitioning using ADI DSP BF609.** The complexity that a Digital Signal Processor handles today is huge. Increasing core complexity or speed is not the only solution. Efficient partitioning of work load between hardware and software is one elegant way of solving this problem. ADI's latest Blackfin DSP solves some of the MIPS hungry algorithms that is typical in imaging and video processing in a very elegant manner by adding accelerating hardware for the tasks which require large number of computations. This will reduce the load on the DSP core, and allows other processing tasks to be implemented very easily.

Mr Prushothaman Palanichamy, Senior Product Marketing Engineer, Xilinx gave a talk on **Open source solutions for the ZYNQ– all programmable SOC.** The Zynq-7000 family combines an ARM® dual-core Cortex™-A9 MPCore™ processing system with programmable logic on a single chip. This architecture allows the device to boot like a processor and load custom hardware or accelerators when the CPU is running. This class of all programmable device gives designers increased flexibility, performance and BOM

cost reduction. But there are challenges in programming this new class of Heterogeneous Systems. The talk was focused on listing the various challenges from Hardware-Software partitioning and addressing these challenges to design an optimized system by leveraging open source or industry standard tools and framework.

Fig. 11 Mr Rajesh Mahapatra, Analog Devices

Fig. 12 Mr Prushothaman Palanichamy, Xilinx

After lunch break, Prof R Govindarajulu, IIIT-H gave a talk on **Growth in Computing Performance.** He explained the developments in hardware and software technologies and the challenges to be addressed with regard to power consumption, user productivity and performance. Future growth in computing must come from parallelism- multicore processors, must use a parallel programming model. Much software is written according to sequential programming model cannot easily be speeded up by using parallel processors. Rethinking programming models is needed, so that programmers can express application parallelism naturally.

Fig. 13 Prof R Govindarajulu, IIIT-H

Fig. 14 Dr Prakash Raghavendra, AMD

Dr. Prakash Raghavendra, Principal Member of Technical Staff, AMD gave a talk on **Aparapi for Java Developers.** Aparapi is an API for expressing data parallel workloads in Java and a runtime component capable of converting the Java byte code of compatible workloads into OpenCL™ so that it can be executed on a variety of GPU devices.

Mr LK Suresh Kumar & Mrs K Shyamala, UCE gave a lecture on **C++ AMP for C++ Developers.** They explained in detail the code-driven C++ Accelerated Massive Parallelism (C++ AMP) that helps C++ developers to understand how the performance can be improved by using parallelism on heterogeneous computing in a hardware portable manner. Few examples for parallelism were also given.

Fig. 15 Mrs Shyamala and Mr Suresh Kumar, UCE

Fig. 16 Prof P Premchand, Dean, UCE during valedictory ceremony

Fig.17 Dr Kiranmai Pendyala, HR Head, AMD

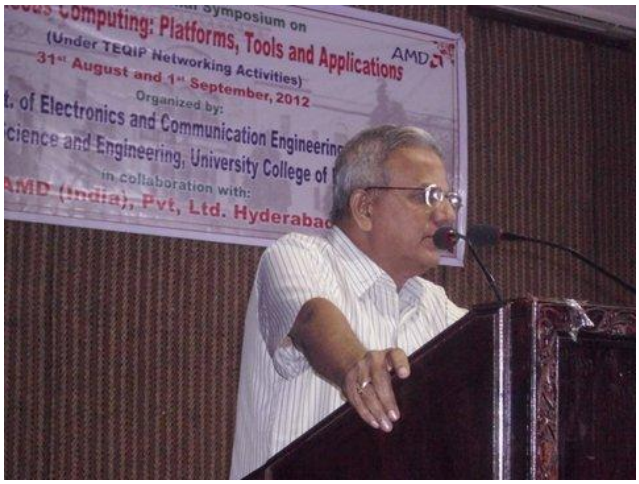

Fig.18 Padmasri N. Divakar, Chairman, Governing Body, UCE

The symposium was concluded with the valedictory function. Padmasri N Divakar, Chairman, UCE Governing Body was the Chief Guest and Dr Kiranmai Pendyala HR Head, AMD India was the Guest of Honor. Dr P Chandrasekhar, HOD, ECE Dept., UCE delivered the opening address and Dr P Laxminarayana, Senior Scientist, NERTU, OU gave the report on the symposium. After that Prof P Premchand, Dean, Faculty of Engineering addressed the audience. Few participants were called on the dais to give feedback about the symposium. One faculty member from ECE Dept., CBIT was very much appreciative of the efforts put forth by UCE for organizing the symposium on the latest trends in the computing with experts from industry, research and academia. Dr Kiranmai said that India has lot of talent and people have to explore it. Shri N Divakar expressed that the faculty, organizations involved in the symposium on Heterogeneous Computing Symposium itself is heterogeneous. He congratulated the faculty and organizers for conducting the symposium. Dr R Hemalatha, faculty member, ECE Dept., UCE gave the vote of thanks. She conveyed thanks on behalf of organizing committee of the symposium, to faculty, staff and students of the departments of the ECE and CSE, AMD management, guest speakers, participants and their respective sponsoring organizations and IETE for providing a nice auditorium. She thanked the ECE Alumni Association, in particular Mr.Navin Rao, Joint Secretary, OUECEAA, for taking initiative and driving various people to make the symposium a grand success.

Fig.19 UCE, ECE & CSE staff &organizers

Fig. 20 Volunteers- UCE, ECE UG and PG students & organizers

Over the two days, 11 guest lectures were delivered. Inaugural and felicitation before lunch on day 1 were organized. The day 2 concluded with valedictory function. Around 250 people registered for the symposium. Approximately 200 participated in addition to 25 faculty members of OU. Among the total participants- 90 were from industry and research organizations and 110 from academia (faculty and students). Around 40 UG/PG ECE students and Mr Navin Rao were very much involved in organizing the event and making it a great success. Special thanks also go to the organizing and advisory committee members of the symposium for their support and guidance.

For more information on the symposium please visit:

UCE website: www.uceou.edu.

AMD developer central: http://developer.amd.com/Resources/IndiaZone/Pages/default.aspx

OU ECE Alumni Association: www.oueceaa.org.